

DECLARATION OF JOINT INVENTORS FOR PATENT APPLICATION

As the below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and joint inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled: Methods of Forming an Isolation Trench in a Semiconductor, Methods of Forming an Isolation Trench in a Surface of a Silicon Wafer, Methods of Forming an Isolation Trench-Isolated Transistor, Trench-Isolated Transistor, Trench Isolation Structures Formed in a Semiconductor, Memory Cells and DRAMS, United States Patent Application Serial No. 09/652,550, filed August 31, 2000.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims.

I acknowledge the duty to disclose information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations §1.56.

PRIOR FOREIGN APPLICATIONS:

I hereby state that no applications for foreign patents or inventor's certificates have been filed prior to the date of execution of this declaration.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and

* * * * *

Full name of inventor: **HIROYUKI WATANABE**

Inventor's Signature: Hiroyuki Watanabe

Date: 10-31-2000

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1 belief are believed to be true; and further that these statements were
2 made with the knowledge that willful false statements and the like so
3 made are punishable by fine or imprisonment, or both, under
4 Section 1001 of Title 18 of the United States Code and that such willful
5 false statement may jeopardize the validity of the application or any
6 patent issued therefrom.

7 * * * * *

8 Full name of inventor: **KEIJI JONO**

9 Inventor's Signature: Keiji Jono

10 Date: 10-31-2000

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16 Full name of inventor: **HIROKAZU UEDA**

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